REMARKS/ARGUMENTS

Favorable reconsideration and allowance of the present application are respectfully requested in view of the following remarks.

A. SUMMARY OF THIS AMENDMENT

By the current amendment, Applicants:

1. Amend claim 2.
2. Respectfully traverse all prior art rejections.

This is in response to the Office Action dated April 17, 2008. Claims 1-13 are pending. Claims 2-4 stand rejected. Claims 1 and 5-13 are allowed. Claim 2 has been amended.

B. PATENTABILITY OF THE CLAIMS

The Examiner's indication that claims 1 and 5-13 are allowed is appreciated. Moreover, it is noted that claim 3 is dependent from claim 1, and as such, it is deemed to be allowable as well.

The rejection of claim 2 under 35 U.S.C. §103(a) as allegedly being unpatentable over Inoue Rieko (JP 09-284572) in view of Iida (2002/0124130), is respectfully traversed.

Amended claim 2 now recites "said image data invalidation unit is configured to store said new image data being input to said device *over a region in which the preceding data is stored*". Support for the amendment can be found, for example, in Fig. 16 of the specification. The combination of Rieko and Iida fails to disclose the above limitation.

Rieko generally discloses an image processing device (Figs. 1-3) comprising an image data input unit 201 for inputting image data [0024], an image data storage unit 304 for storing the image data input through the image data input unit [0047], an image data processing unit 204 for processing the image data stored in the image data storage unit [0050]. Furthermore, Rieko's system includes an image data invalidation unit for invalidating data stored in the storage unit 304 [0051]-[0056]. This unit may receive a request for "elimination stop", in which case the image data is not deleted. The Examiner acknowledged that Rieko fails to teach that when there is input of a new image data through the image data input unit after a preceding image data has been processed but before the image data invalidation unit has started the invalidation of the preceding image data, the image data invalidation unit stores the new image data. He then resorted to Iida for the missing limitations.

Iida discloses a flash memory [0060]. The flash memory comprises segment(s), each segment divided into blocks, each block further divided into multiple pages, Fig. 7, [0071]-[0076]. Data is written into and read out from the flash memory in page units. However, data is erased from a flash memory in block units. Moreover, a flash memory is characterized in that data can not be written into an area in which other data has already been written before. Therefore, before writing data into a block, it is necessary to erase the contents thereof [0079].

The Examiner stated that Iida discloses a memory controller where new data is written into the memory block and the old data is then deleted from the occupied block (citing claim 8 in Iida). Therefore, he asserted that it would have been obvious to one of ordinary skill to use such memory controller in Rieko's image processing unit to enhance storing new image data and deleting the old.

With the amendment to claim 2, it is made clear that the new image data is written in a region where the preceding image data is written. This can not happen in the flash memory of Iida, where new data is only written in areas where older data does not exist (either because it was never written or because it has been deleted, see [0079]).

Moreover, in the flash memory of Iida, old data must first be deleted and then new data can be stored (see for example, [0079], [0183], [0190]). Claim 8, cited by the Examiner, recites "said new data is written into an unused block and said old data is deleted from said occupied block". However, "unused" block is defined in claim 6, from which claim 8 depends, as "a block from which data was deleted". In other words, according to claim 8, new data can not be written in a block until the old data is deleted thereof.

Therefore, Iida fails to teach "when there is input of a new image data through said image data input unit after a preceding image data has been processed but before said image data invalidation unit has started the invalidation of said preceding image data stored in said image data storage unit". In other words, in Iida's memory, storing of new data must follow deletion of old data, which is opposite to the claimed sequence of events.

For the above reasons, claim 2 is allowable.

It is respectfully requested that the rejection of claim 4, which is dependent from claim 2, also be withdrawn.

C. MISCELLANEOUS

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

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